MDX-C6400R/C6500R/C6500RX

SERVICE MANUAL

Ver 1.1 2001.05

AEP Model

MDX-C6400R/C6500R/C6500RX

UK Model

MDX-C6500R/C6500RX

Photo: MDX-C6500R

Model Name Using Similar Mechanism	NEW
Base Mechanism Type	MG-164NZ-138
Optical Pick-up Name	KMS-241C/J1NP

SPECIFICATIONS

MD player section

Signal-to-noise ratio	90 dB
Frequency response	10 – 20,000 Hz
Wow and flutter	Below measurable limit

Tuner section

FM

Tuning range	87.5 – 108.0 MHz
Aerial terminal	External aerial connector
Intermediate frequency	10.7 MHz/450 kHz
Usable sensitivity	8 dBf
Selectivity	75 dB at 400 kHz
Signal-to-noise ratio	66 dB (stereo), 72 dB (mono)
Harmonic distortion at 1 kHz	0.6 % (stereo), 0.3 % (mono)
Separation	35 dB at 1 kHz
Frequency response	30 – 15,000 Hz

MW/LW

Tuning range	MW: 531 – 1,602 kHz LW: 153 – 279 kHz
Aerial terminal	External aerial connector
Intermediate frequency	10.7 MHz/450 kHz
Sensitivity	MW: 30 µV LW: 40 µV

Power amplifier section

Outputs	Speaker outputs (sure seal connectors)
Speaker impedance	4 – 8 ohms
Maximum power output	50 W × 4 (at 4 ohms)

General

Outputs	Audio outputs*1 Power aerial relay control lead Power amplifier control lead Telephone ATT control lead*2
Tone controls	Bass ±9 dB at 100 Hz Treble ±9 dB at 10 kHz
Power requirements	12 V DC car battery (negative ground)
Dimensions	Approx. 178 × 50 × 183 mm (w/h/d)
Mounting dimensions	Approx. 182 × 53 × 162 mm (w/h/d)
Mass	Approx. 1.2 kg
Supplied accessories	Parts for installation and connections (1 set) Front panel case (1)

*1 *Equipped with front and rear outputs: MDX-C6500RX/C6500R only*
Equipped with rear outputs: MDX-C6400R

*2 *MDX-C6500RX/C6500R only*

U.S. and foreign patents licensed from Dolby laboratories Licensing Corporation.

Design and specifications are subject to change without notice.

FM/MW/LW MINIDISC PLAYER

9-870-051-12
2001E0500-1

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Shinagawa Tec Service Manual Production Group

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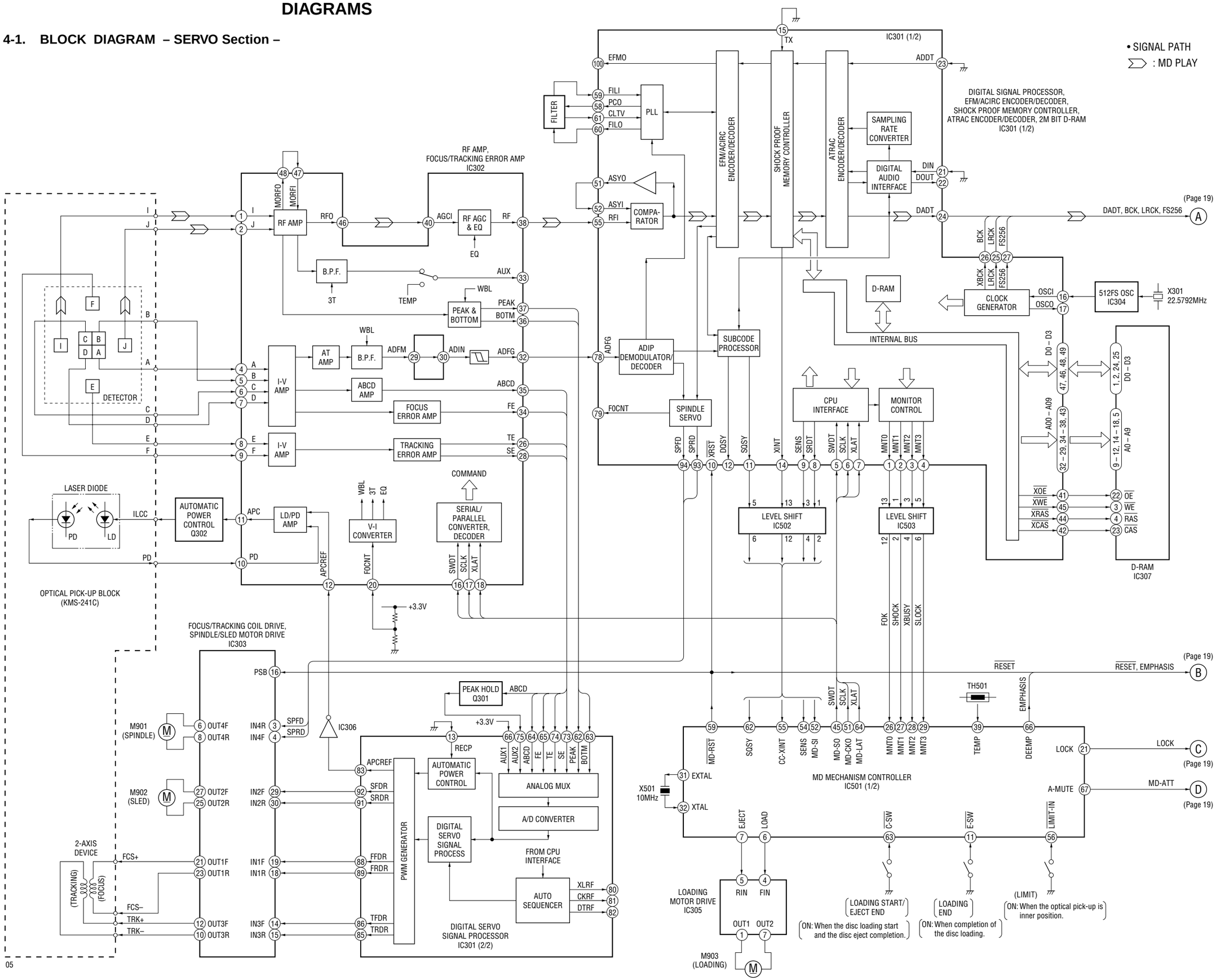
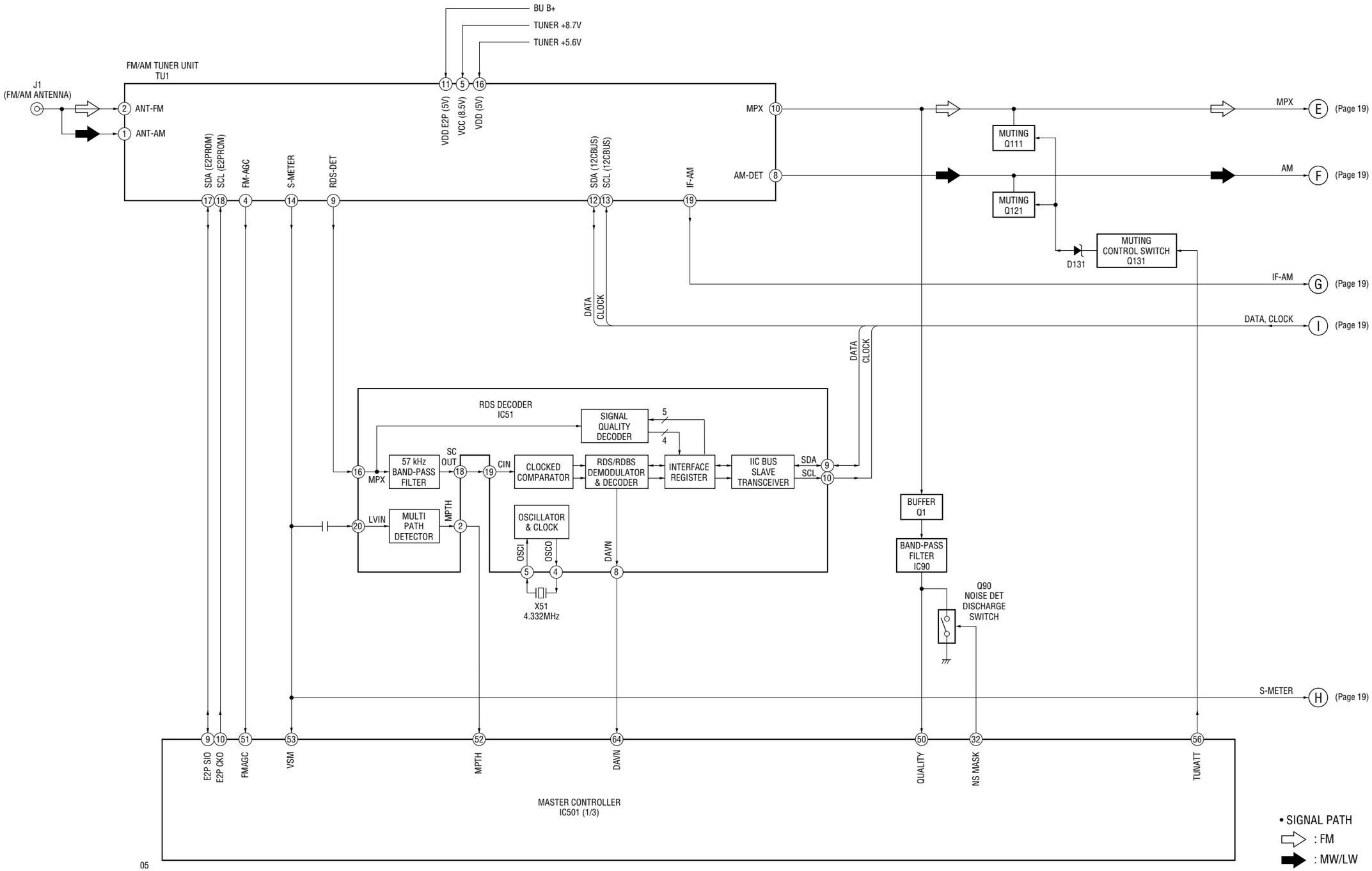
SECTION 4
DIAGRAMS

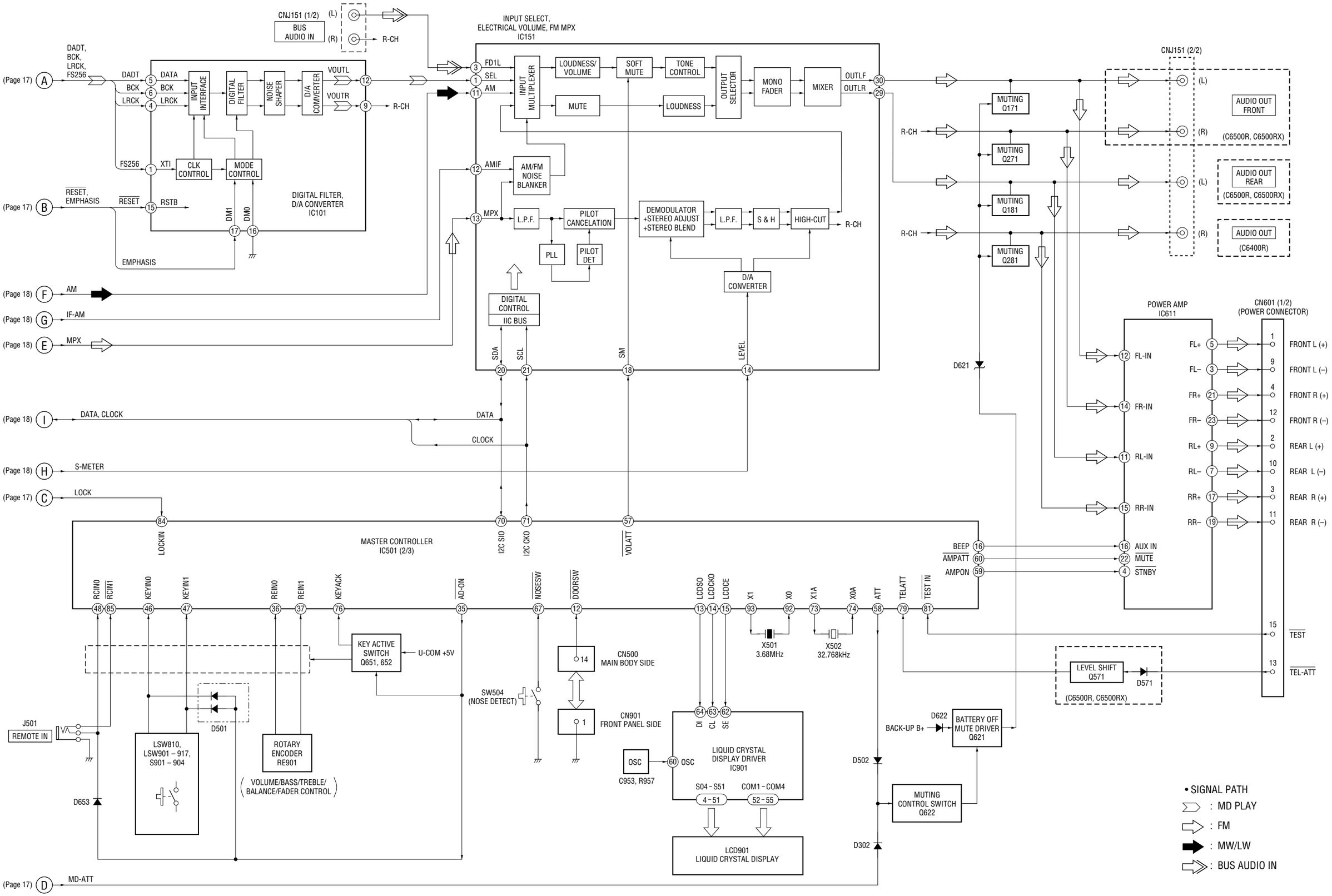
4-1. BLOCK DIAGRAM – SERVO Section –



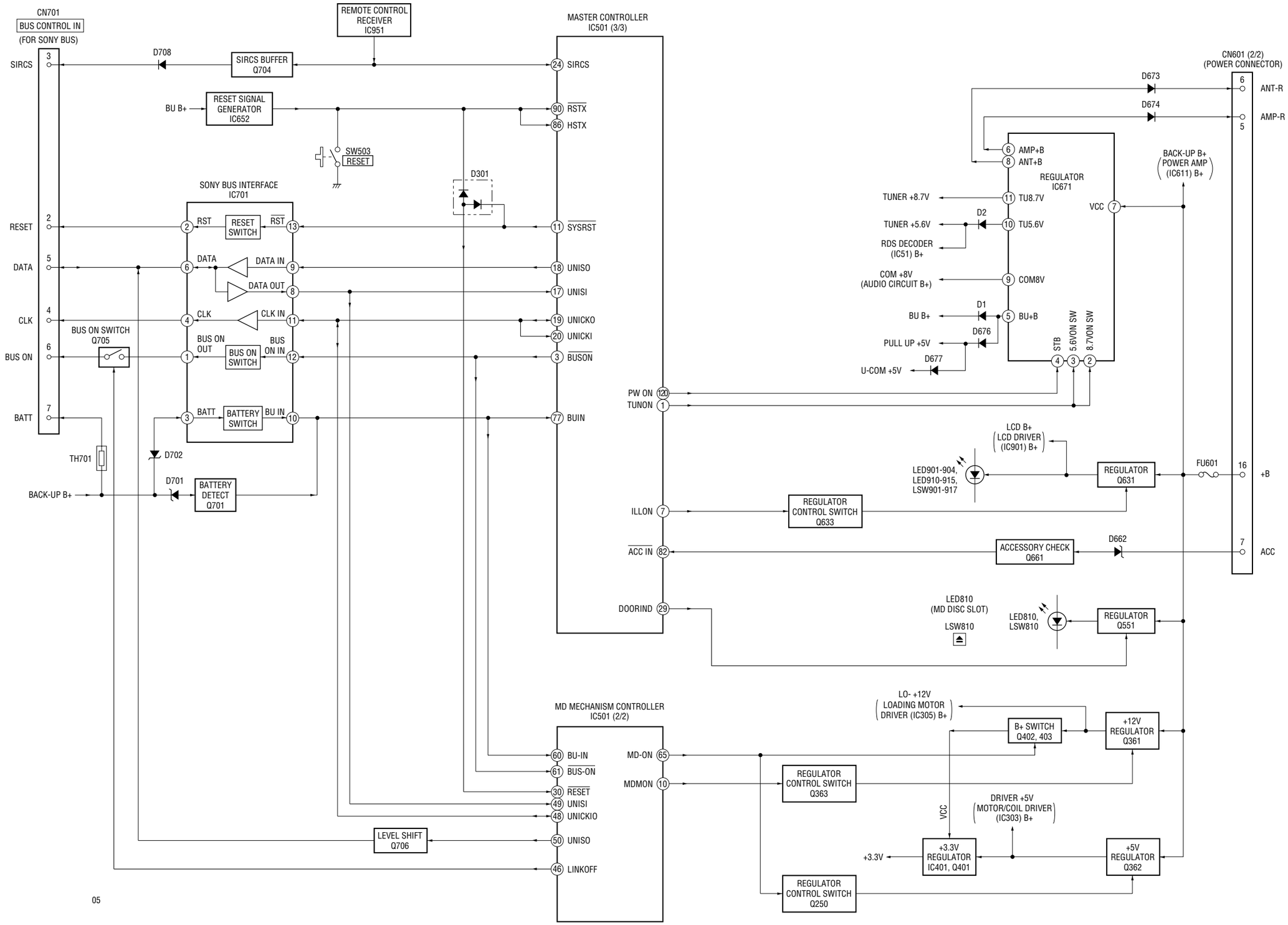
4-2. BLOCK DIAGRAM – TUNER Section –



4-3. BLOCK DIAGRAM – MAIN Section –

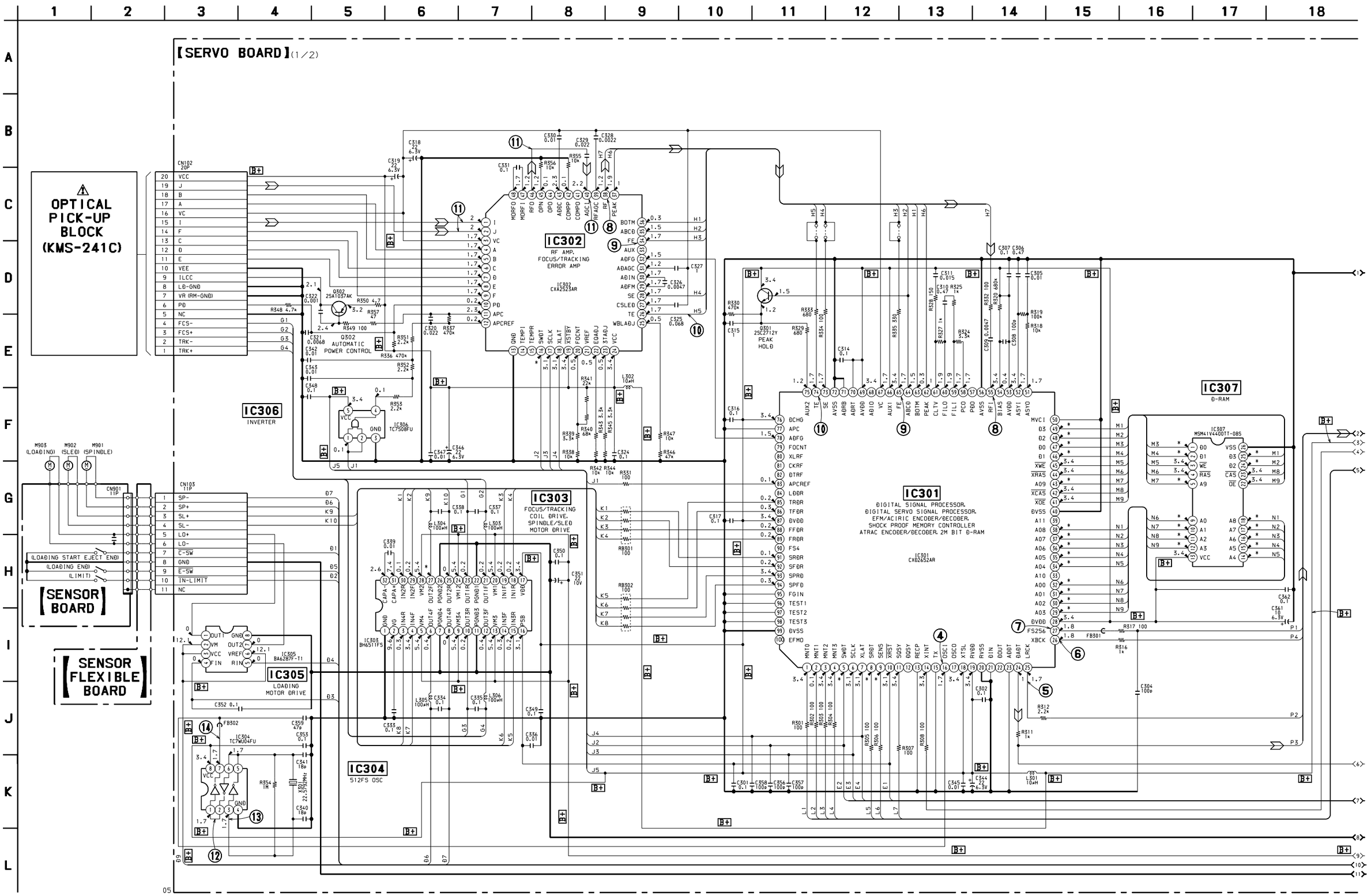


4-4. BLOCK DIAGRAM – BUS CONTROL/POWER SUPPLY Section –



4-8. SCHEMATIC DIAGRAM – SERVO Board (1/2) –

• See page 31 for Waveforms. • See page 36 for IC Block Diagrams.



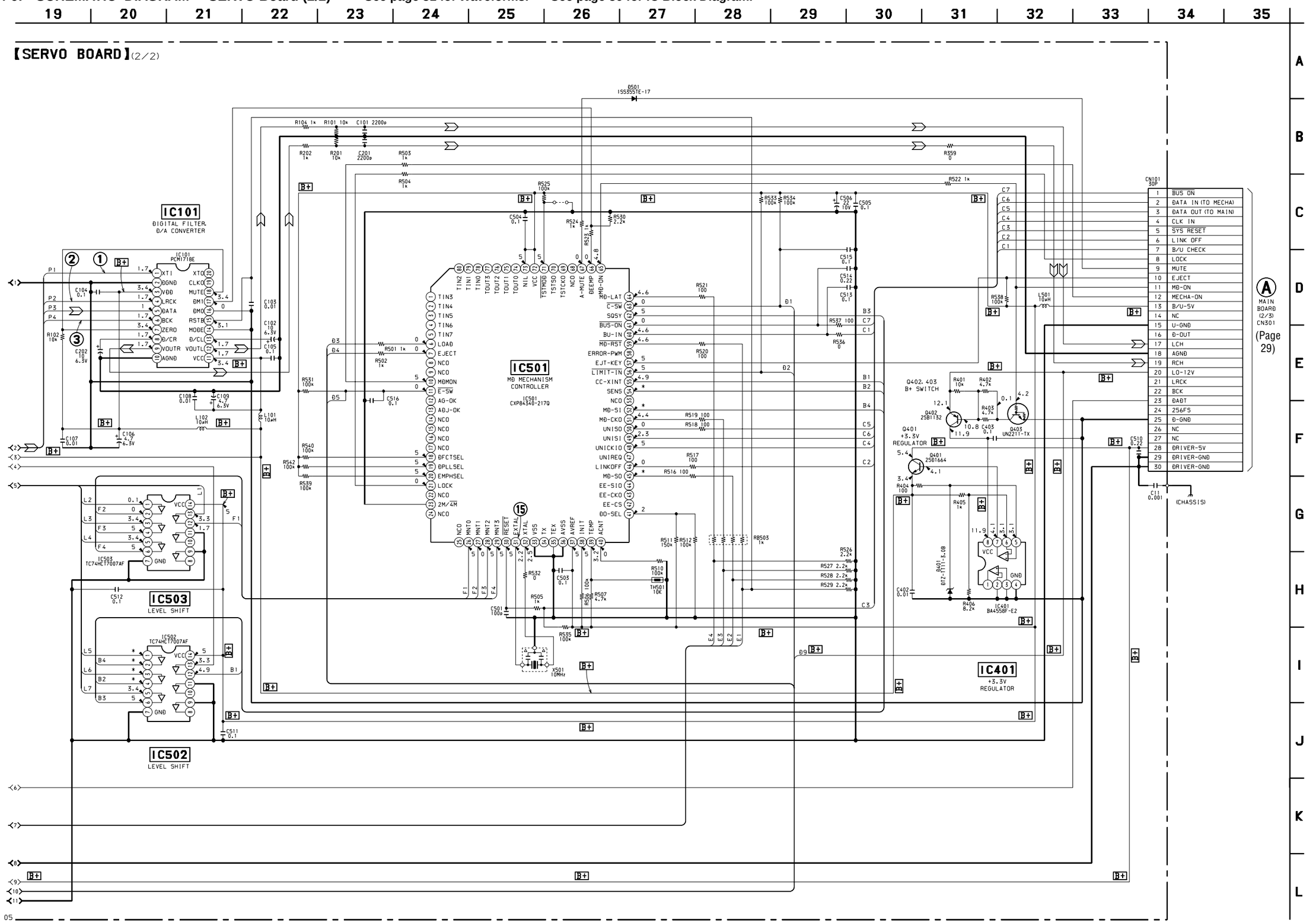
- Voltages and waveforms are dc with respect to ground under no-signal conditions.
  no mark : MD PLAY
  ∗ : Impossible to measure

The components identified by mark ⚠ or dotted line with mark ⚠ are critical for safety.
Replace only with part number specified.

4-9. SCHEMATIC DIAGRAM – SERVO Board (2/2) –

• See page 31 for Waveforms. • See page 36 for IC Block Diagram.

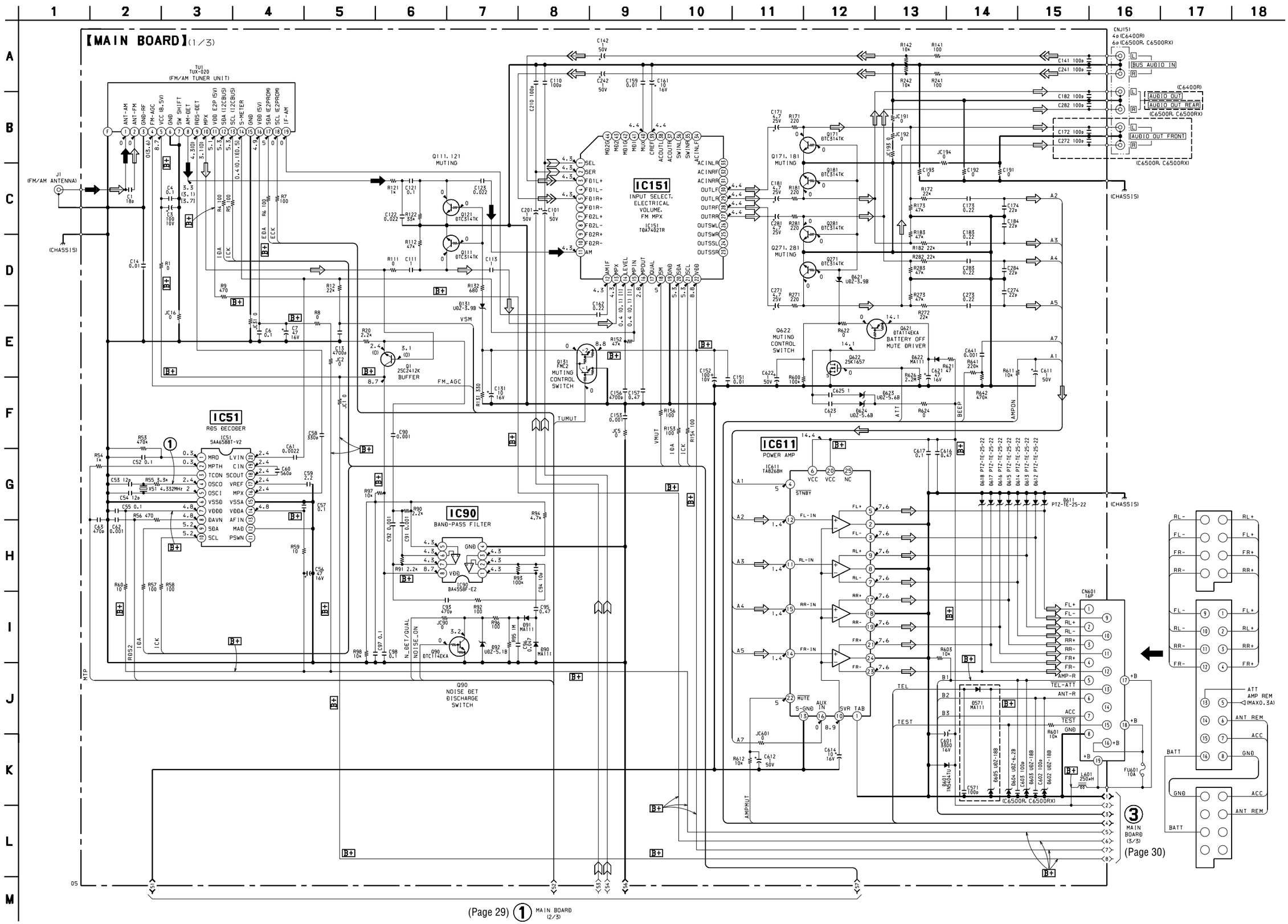
【SERVO BOARD】(2/2)



- Voltages and waveforms are dc with respect to ground under no-signal conditions.
  no mark : MD PLAY
  ∗ : Impossible to measure

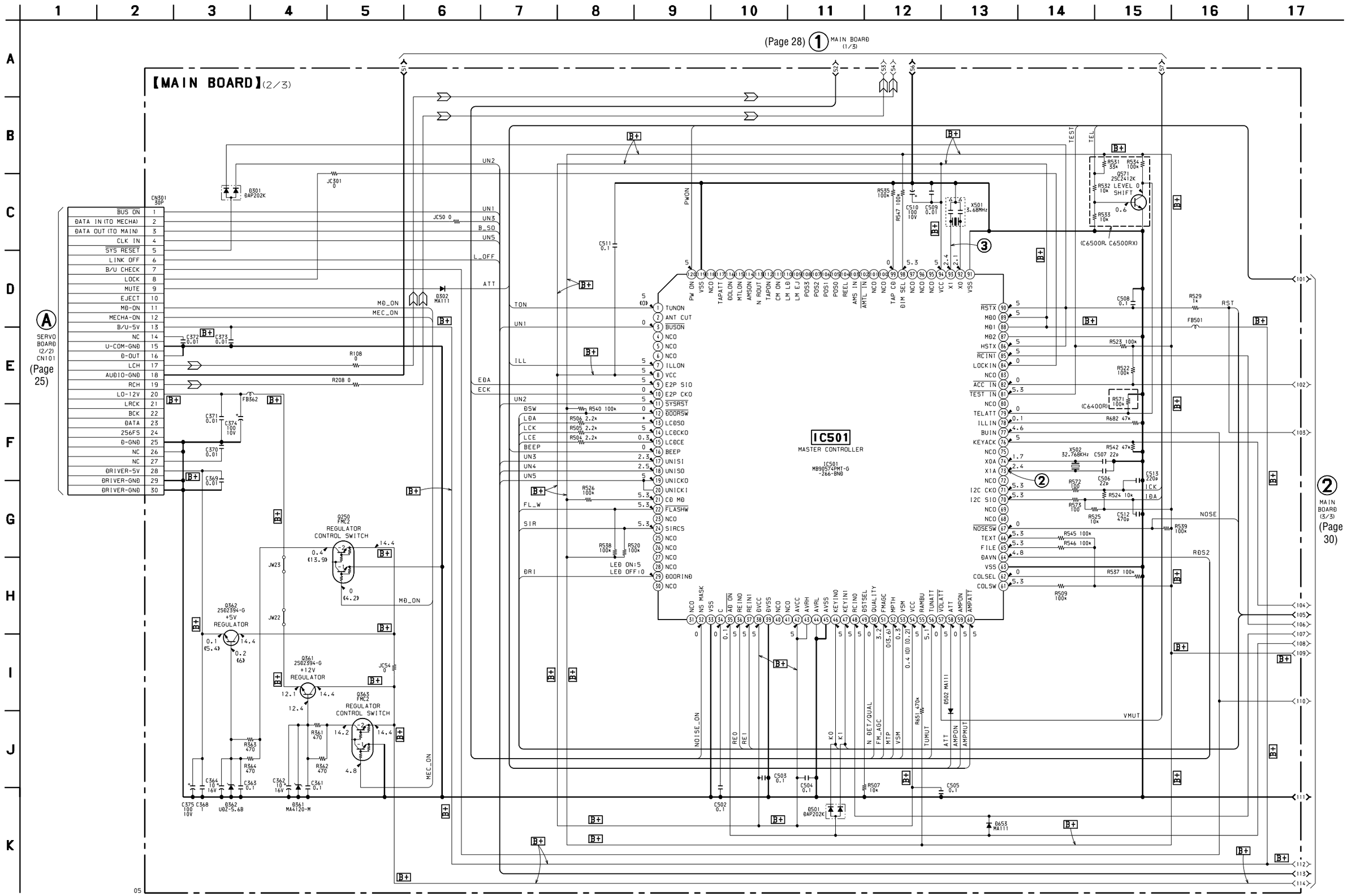
4-12. SCHEMATIC DIAGRAM – MAIN Board (1/3) –

• See page 31 for Waveform. • See page 36 for IC Block Diagrams.



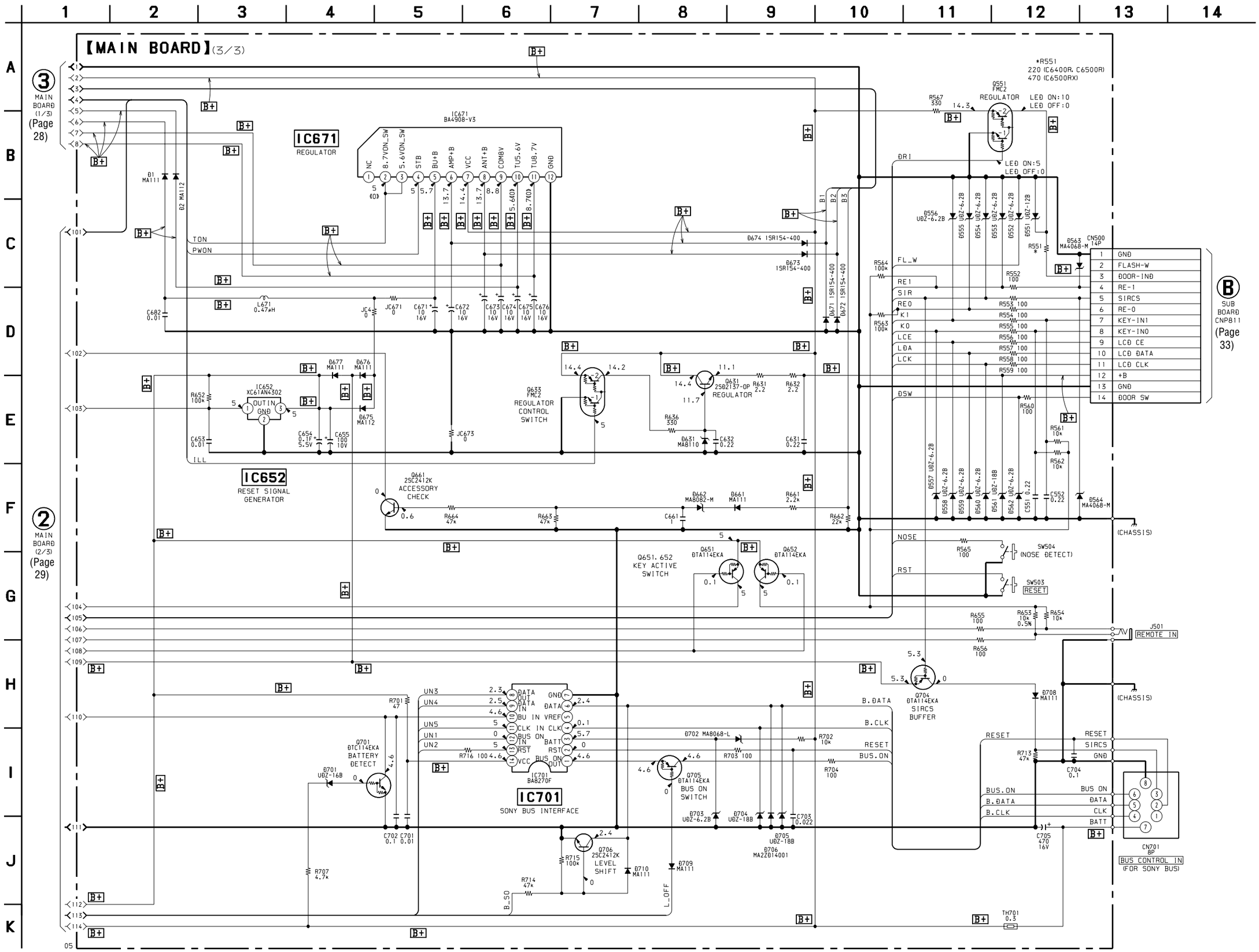
- Voltages and waveforms are dc with respect to ground under no-signal (detuned) conditions.
  no mark : FM
  ( ) : MW
  [ ] : LW

4-13. SCHEMATIC DIAGRAM – MAIN Board (2/3) – • See page 31 for Waveforms.

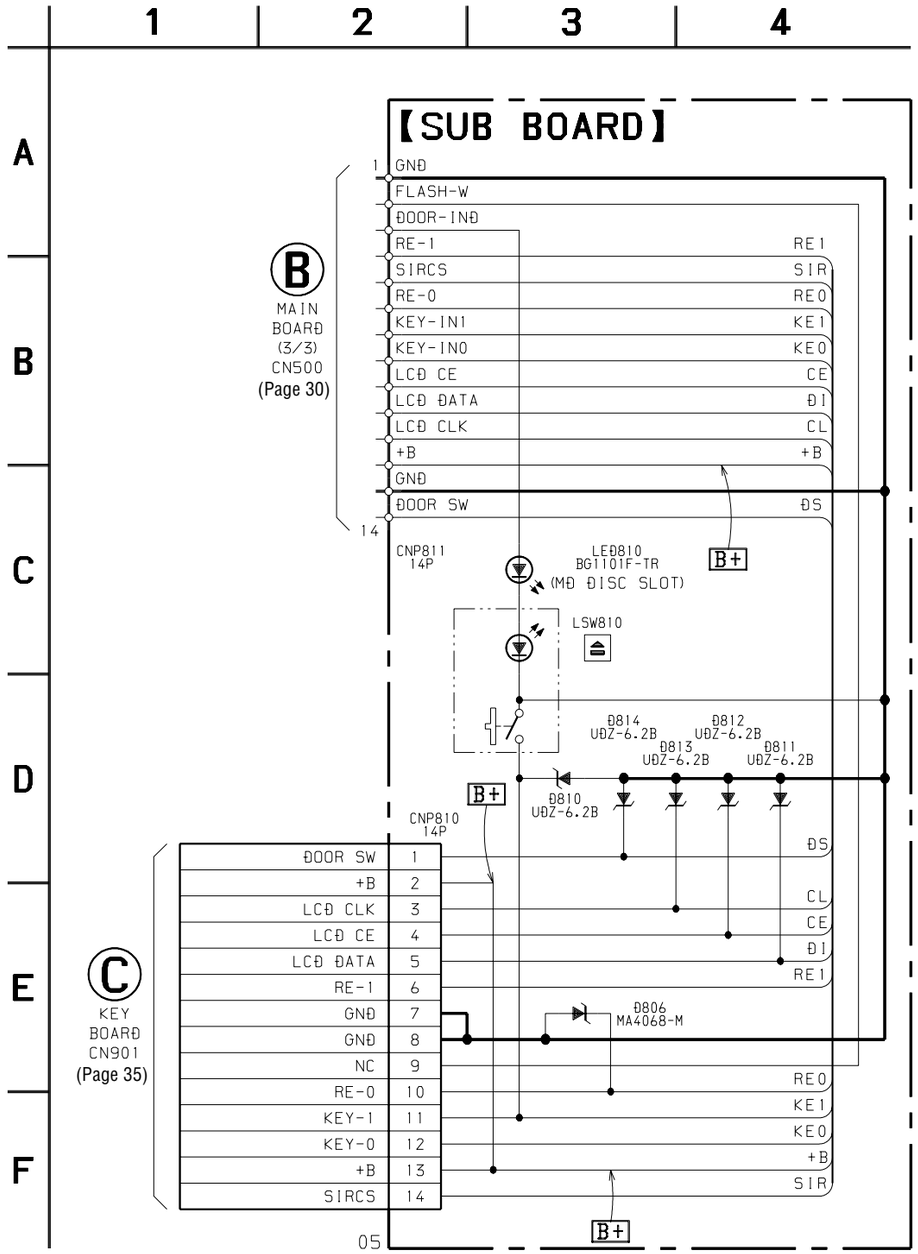


- Voltages and waveforms are dc with respect to ground under no-signal (detuned) conditions.
  no mark : FM
  ( ) : MW
  [ ] : LW
  ⟨⟨ ⟩⟩ : MD PLAY
  * : Impossible to measure

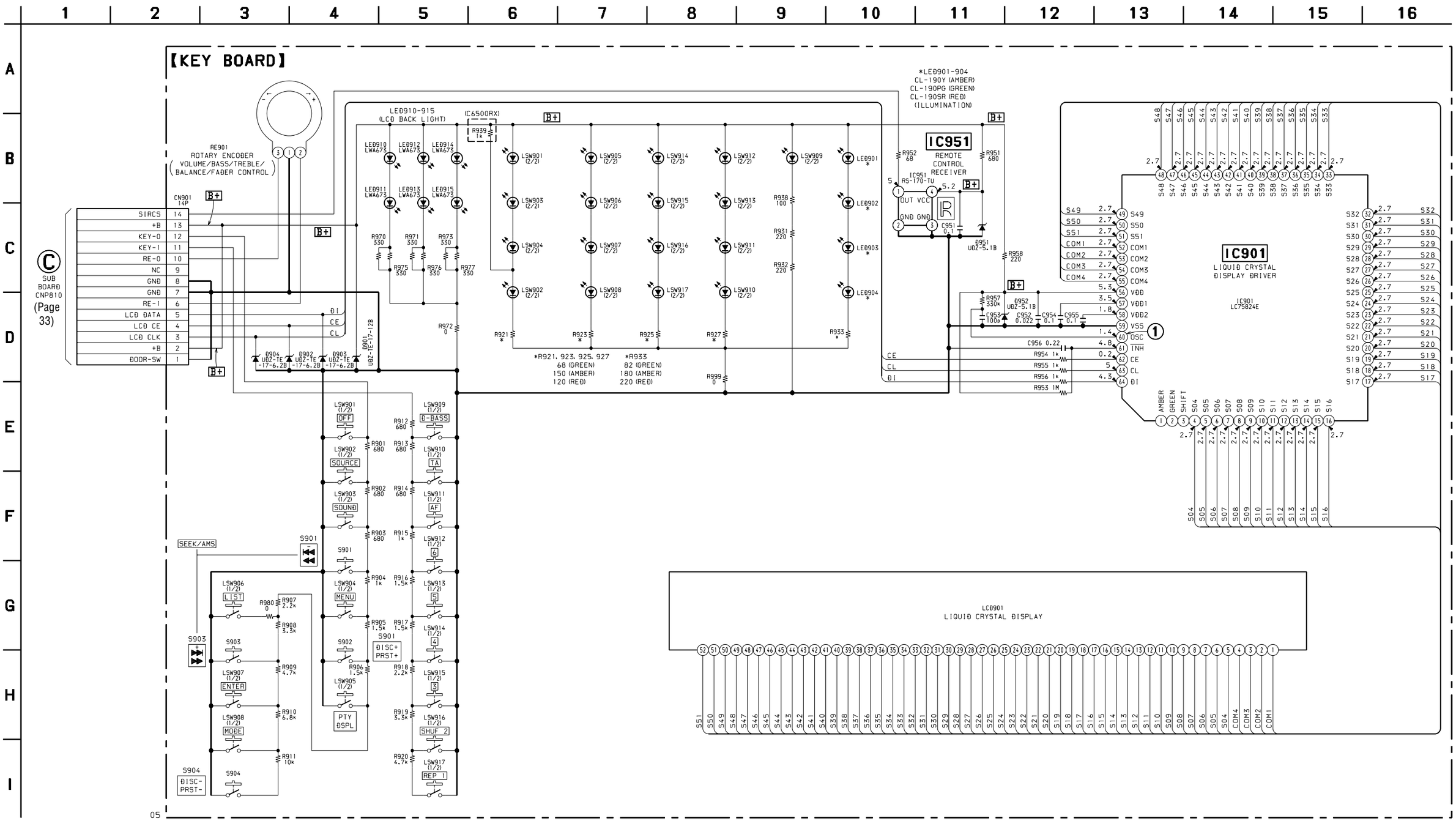
4-14. SCHEMATIC DIAGRAM – MAIN Board (3/3) – • See page 36 for IC Block Diagrams.



- Voltages are dc with respect to ground under no-signal (detuned) conditions.
  no mark : FM
  ⟨⟨ ⟩⟩ : MD PLAY


1
2
3
4
A
B
C
D
E
F
【SUB BOARD】
1 GND
FLASH-W
DOOR-IND
RE-1
SIRCS
RE-0
KEY-IN1
KEY-IN0
LCD CE
LCD DATA
LCD CLK
+B
GND
DOOR SW
14
B
MAIN BOARD (3/3) CN500 (Page 30)
RE1
SIR
RE0
KE1
KE0
CE
DI
CL
+B
DS
CNP811 14P
LED810 BG1101F-TR
(MD DISC SLOT)
B+
LSW810
D814 UDZ-6.2B
D812 UDZ-6.2B
D813 UDZ-6.2B
D811 UDZ-6.2B
D810 UDZ-6.2B
CNP810 14P
DOOR SW 1
+B 2
LCD CLK 3
LCD CE 4
LCD DATA 5
RE-1 6
GND 7
GND 8
NC 9
RE-0 10
KEY-1 11
KEY-0 12
+B 13
SIRCS 14
C
KEY BOARD CN901 (Page 35)
D806 MA4068-M
05

4-18. SCHEMATIC DIAGRAM – KEY Board – • See page 31 for Waveform.

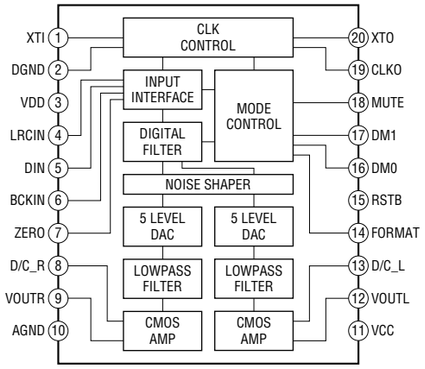


- Voltages and waveforms are dc with respect to ground under no-signal (detuned) conditions.
  no mark : FM

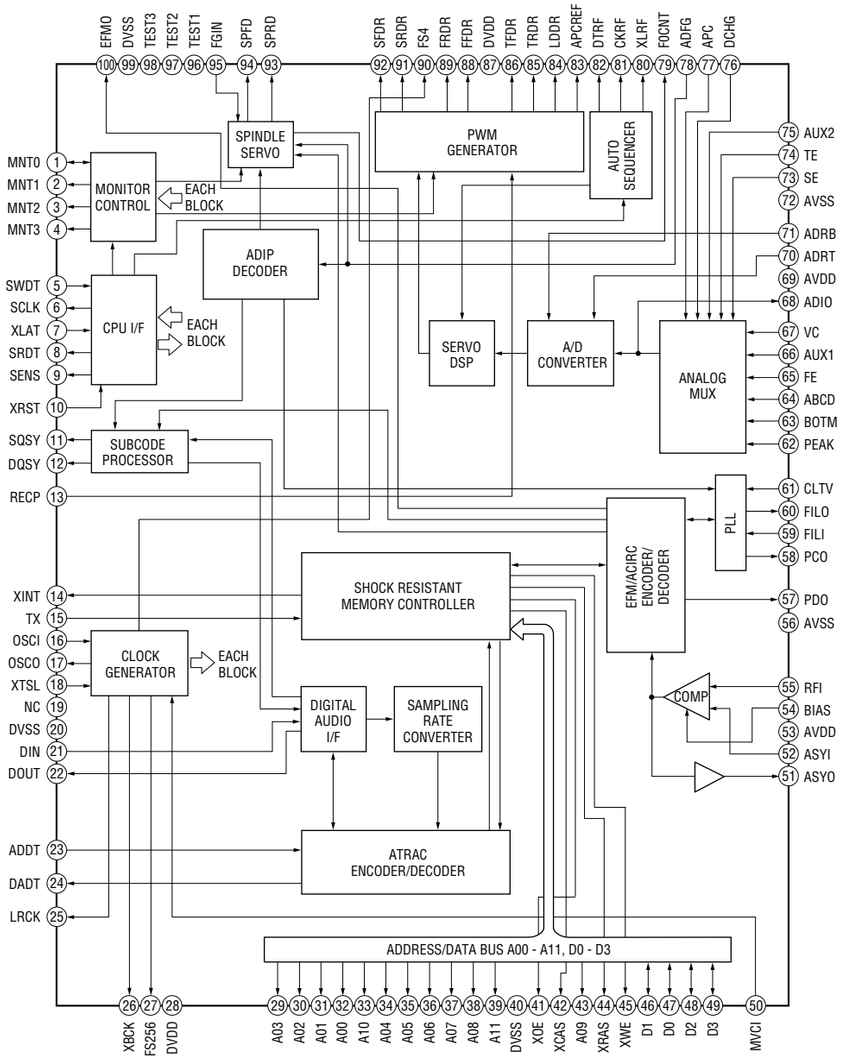
• **IC Block Diagrams**

– SERVO Board –

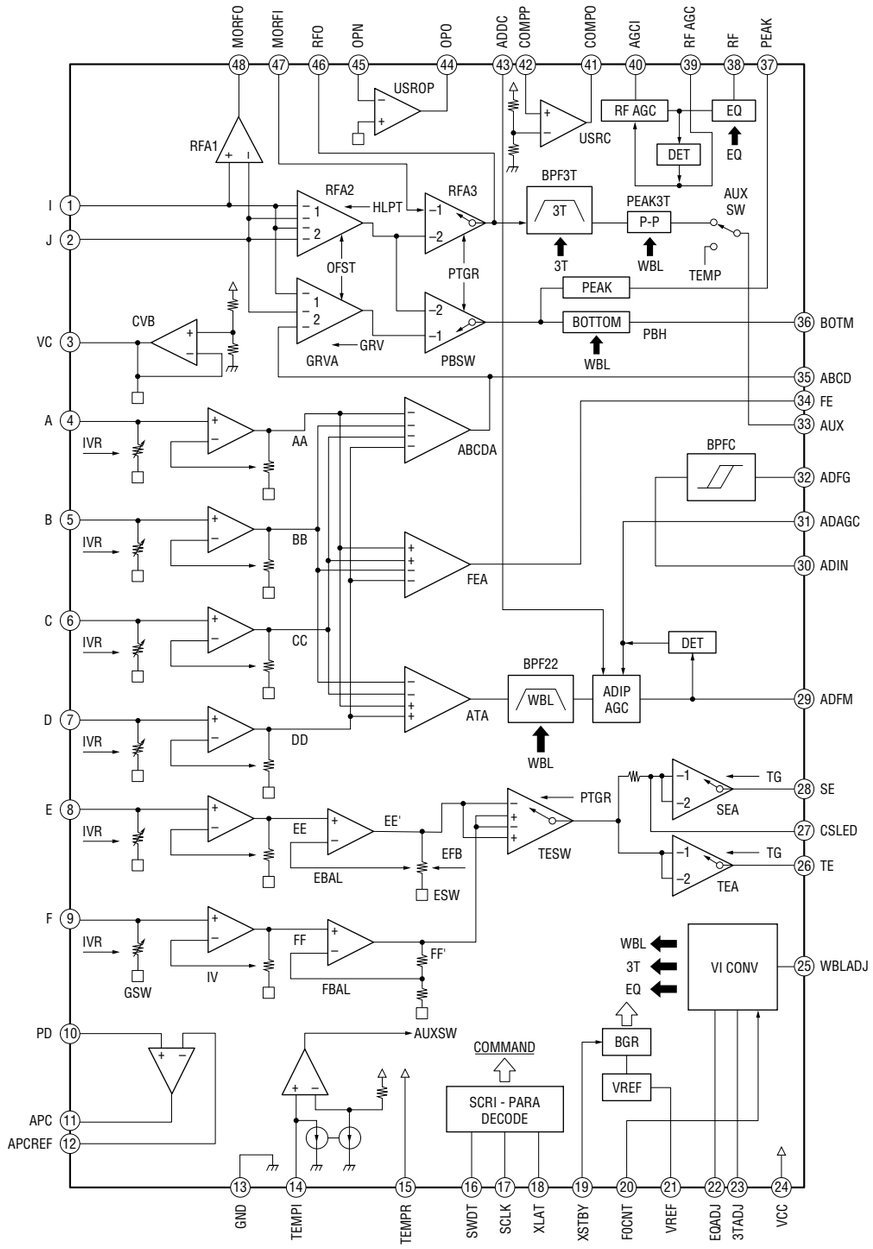
IC101 PCM1718E/2K



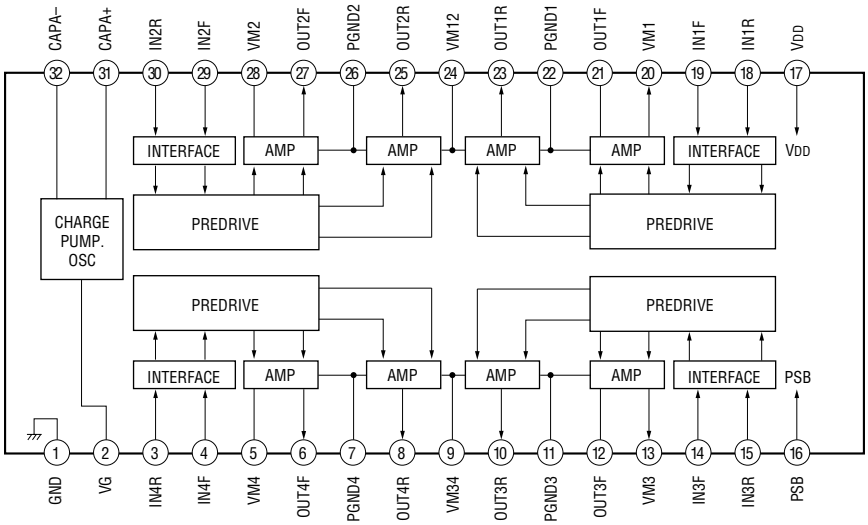
IC301 CXD2652AR



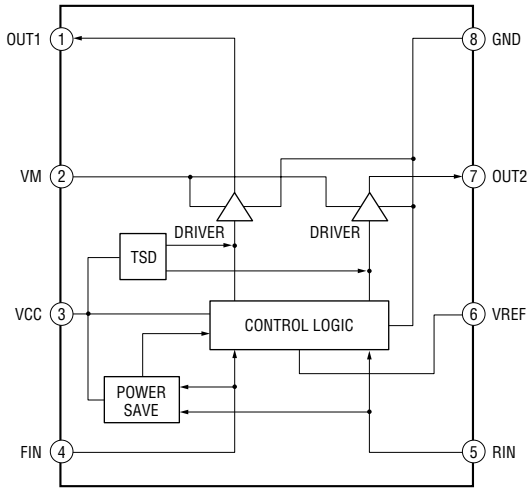
IC302 CXA2523AR



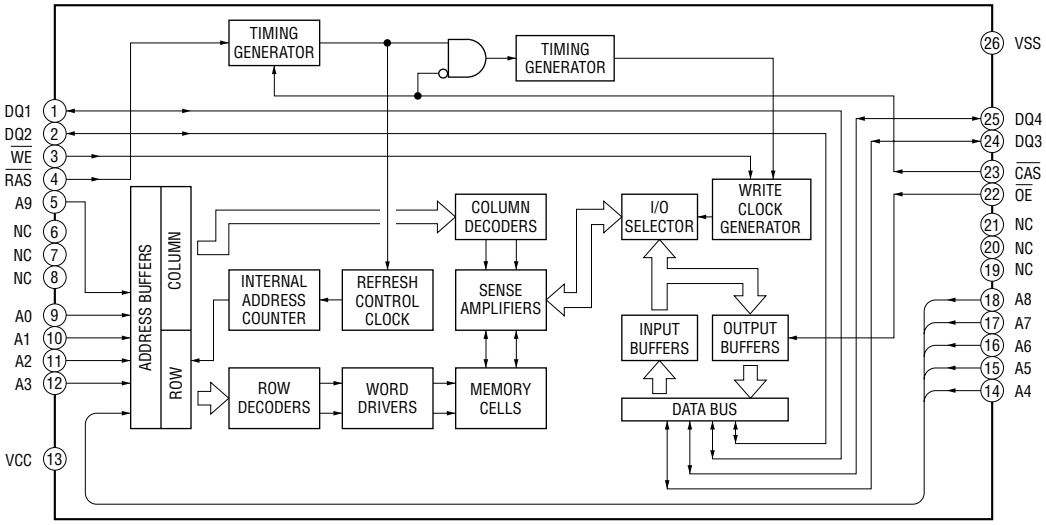
IC303 BH6511FS-E2



IC305 BA6287F

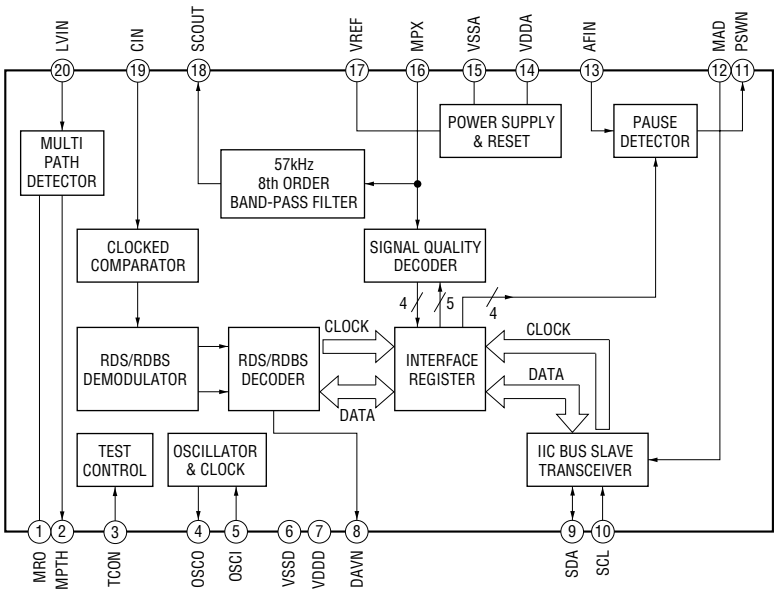


IC307 MN41V4400TT-08S

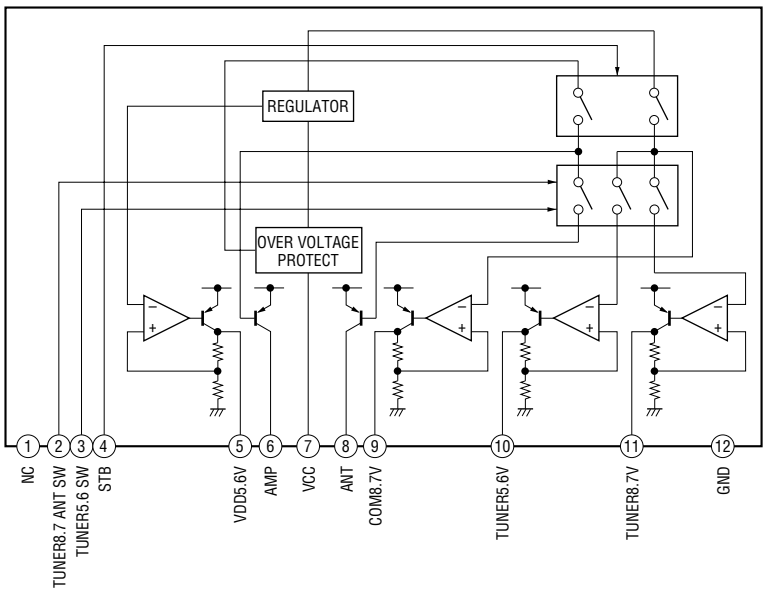


– MAIN Board –

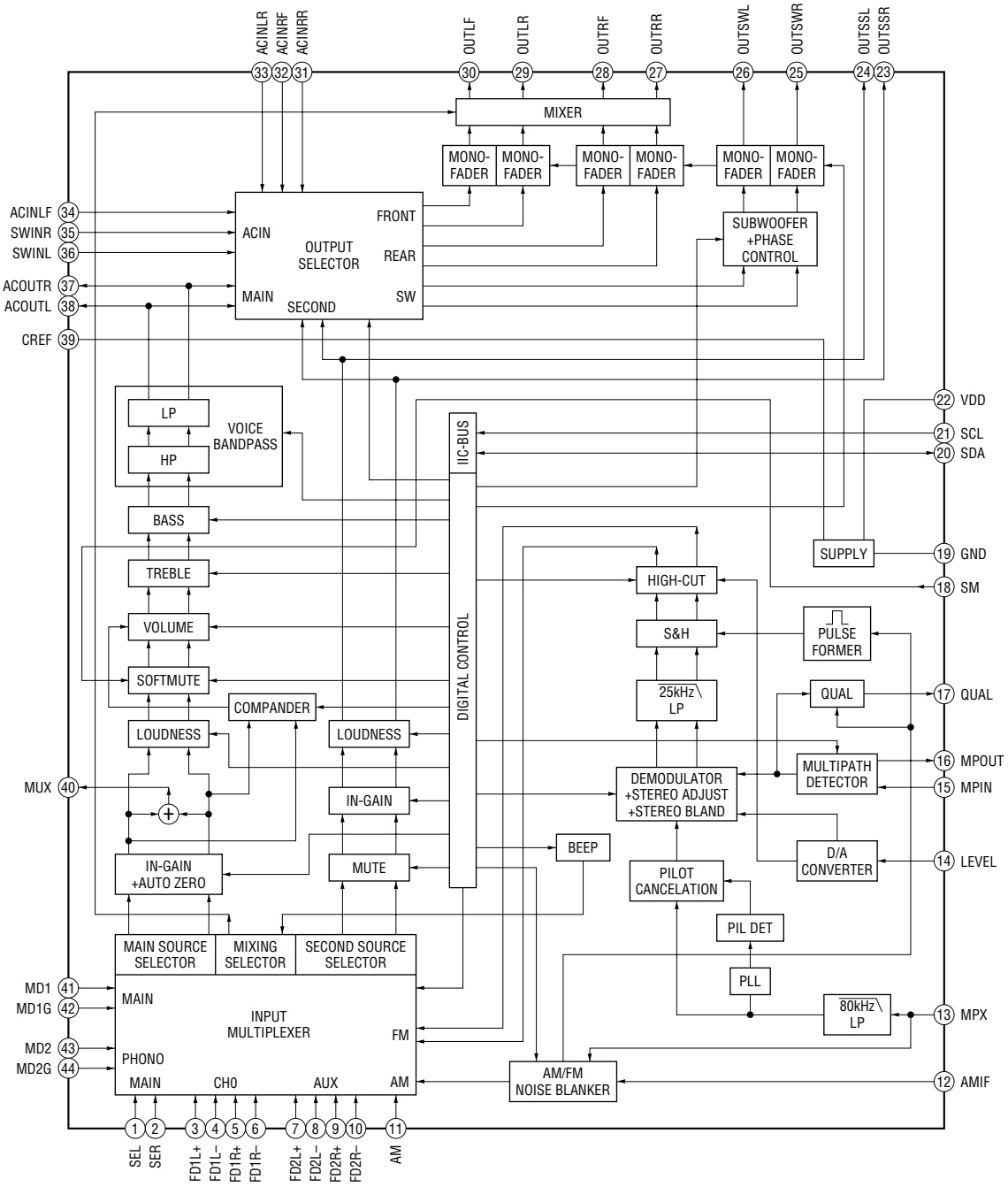
IC51 SAA6588T/V2-118



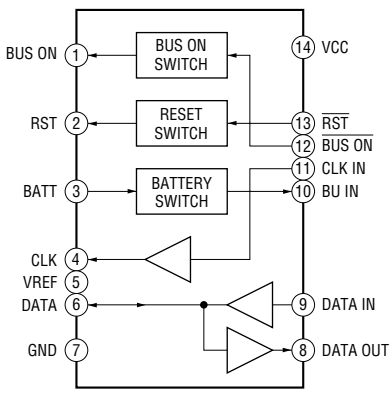
IC671 BA4908-V3



IC151 TDA7402TR



IC701 BA8270F-E2



4-19. IC PIN FUNCTION DESCRIPTION

- **SERVO BOARD IC301 CXD2652AR**
  (DIGITAL SIGNAL PROCESSOR, DIGITAL SERVO PROCESSOR, EFM/ACIRC ENCODER/DECODER, SHOCK PROOF MEMORY CONTROLLER, ATRAC ENCODER/DECODER, 2M BIT D-RAM)

Pin No.	Pin Name	I/O	Description
1	MNT0	O	Focus OK signal output to the MD mechanism controller (IC501) "H" is output when focus is on ("L": NG)
2	MNT1	O	Track jump detection signal output to the MD mechanism controller (IC501)
3	MNT2	O	Busy monitor signal output to the MD mechanism controller (IC501)
4	MNT3	O	Spindle servo lock status monitor signal output to the MD mechanism controller (IC501)
5	SWDT	I	Writing serial data signal input from the MD mechanism controller (IC501)
6	SCLK	I	Serial data transfer clock signal input from the MD mechanism controller (IC501)
7	XLAT	I	Serial data latch pulse signal input from the MD mechanism controller (IC501)
8	SRDT	O (3)	Reading serial data signal output to the MD mechanism controller (IC501)
9	SENS	O (3)	Internal status (SENSE) output to the MD mechanism controller (IC501)
10	$\overline{\text{XRST}}$	I	Reset signal input from the MD mechanism controller (IC501) "L": reset
11	SQSY	O	Subcode Q sync (SCOR) output to the MD mechanism controller (IC501) "L" is output every 13.3 msec Almost all, "H" is output
12	DQSY	O	Digital In U-bit CD format subcode Q sync (SCOR) output terminal "L" is output every 13.3 msec Almost all, "H" is output Not used (open)
13	RECP	I	Laser power selection signal input terminal "L": playback mode, "H": recording mode (fixed at "L" in this set)
14	XINT	O	Interrupt status output to the MD mechanism controller (IC501)
15	TX	I	Recording data output enable signal input terminal Writing data transmission timing input (Also serves as the magnetic head on/off output) Not used (fixed at "L")
16	OSCI	I	System clock signal (512Fs=22.5792 MHz) input from the oscillator circuit
17	OSCO	O	System clock signal (512Fs=22.5792 MHz) output terminal Not used (open)
18	XTSL	I	Input terminal for the system clock frequency setting "L": 45.1584 MHz, "H": 22.5792 MHz (fixed at "H" in this set)
19	RVDD	—	Power supply terminal (+3.3V) (digital system)
20	RVSS	—	Ground terminal (digital system)
21	DIN	I	Digital audio signal input terminal when recording mode Not used (fixed at "L")
22	DOUT	O	Digital audio signal output terminal when playback mode Not used (open)
23	ADDT	I	Recording data input terminal Not used (fixed at "L")
24	DADT	O	Playback data output to the PCM1718E (IC101)
25	LRCK	O	L/R sampling clock signal (44.1 kHz) output to the PCM1718E (IC101)
26	XBCK	O	Bit clock signal (2.8224 MHz) output to the PCM1718E (IC101)
27	FS256	O	Clock signal (11.2896 MHz) output to the PCM1718E (IC101)
28	DVDD	—	Power supply terminal (+3.3V) (digital system)
29 to 32	A03 to A00	O	Address signal output to the D-RAM (IC307)
33	A10	O	Address signal output to the external D-RAM Not used (open)
34 to 38	A04 to A08	O	Address signal output to the D-RAM (IC307)
39	A11	O	Address signal output to the external D-RAM Not used (open)
40	DVSS	—	Ground terminal (digital system)
41	$\overline{\text{XOE}}$	O	Output enable signal output to the D-RAM (IC307) "L" active
42	$\overline{\text{XCAS}}$	O	Column address strobe signal output to the D-RAM (IC307) "L" active
43	A09	O	Address signal output to the D-RAM (IC307)
44	$\overline{\text{XRAS}}$	O	Row address strobe signal output to the D-RAM (IC307) "L" active
45	$\overline{\text{XWE}}$	O	Write enable signal output to the D-RAM (IC307) "L" active

Pin No.	Pin Name	I/O	Description
46	D1	I/O	Two-way data bus with the D-RAM (IC307)
47	D0	I/O	
48	D2	I/O	
49	D3	I/O	
50	MVCI	I	Digital in PLL oscillation input from the external VCO Not used (fixed at “L”)
51	ASYO	O	Playback EFM full-swing output terminal
52	ASYI	I (A)	Playback EFM asymmetry comparator voltage input terminal
53	AVDD	—	Power supply terminal (+3.3V) (analog system)
54	BIAS	I (A)	Playback EFM asymmetry circuit constant current input terminal
55	RFI	I (A)	Playback EFM RF signal input from the CXA2523AR (IC302)
56	AVSS	—	Ground terminal (analog system)
57	PDO	O (3)	Phase comparison output for clock playback analog PLL of the playback EFM Not used (open)
58	PCO	O (3)	Phase comparison output for master clock of the recording/playback EFM master PLL
59	FILI	I (A)	Filter input for master clock of the recording/playback master PLL
60	FILO	O (A)	Filter output for master clock of the recording/playback master PLL
61	CLTV	I (A)	Internal VCO control voltage input of the recording/playback master PLL
62	PEAK	I (A)	Light amount signal (RF/ABCD) peak hold input from the CXA2523AR (IC302)
63	BOTM	I (A)	Light amount signal (RF/ABCD) bottom hold input from the CXA2523AR (IC302)
64	ABCD	I (A)	Light amount signal (ABCD) input from the CXA2523AR (IC302)
65	FE	I (A)	Focus error signal input from the CXA2523AR (IC302)
66	AUX1	I (A)	Auxiliary signal (I_3 signal/temperature signal) input terminal Not used (fixed at “H”)
67	VC	I (A)	Middle point voltage (+1.65V) input from the CXA2523AR (IC302)
68	ADIO	O (A)	Monitor output of the A/D converter input signal Not used (open)
69	AVDD	—	Power supply terminal (+3.3V) (analog system)
70	ADRT	I (A)	A/D converter operational range upper limit voltage input terminal (fixed at “H” in this set)
71	ADRB	I (A)	A/D converter operational range lower limit voltage input terminal (fixed at “L” in this set)
72	AVSS	—	Ground terminal (analog system)
73	SE	I (A)	Sled error signal input from the CXA2523AR (IC302)
74	TE	I (A)	Tracking error signal input from the CXA2523AR (IC302)
75	AUX2	I (A)	Auxiliary signal input terminal Light amount signal input from the CXA2523AR (IC302)
76	DCHG	I (A)	Connected to the +3.3V power supply
77	APC	I (A)	Error signal input for the laser automatic power control Not used (fixed at “L”)
78	ADFG	I	ADIP duplex FM signal (22.05 kHz ± 1 kHz) input from the CXA2523AR (IC302)
79	F0CNT	O	Filter f0 control signal output terminal Not used (open)
80	XLRF	O	Serial data latch pulse signal output terminal Not used (open)
81	CKRF	O	Serial data transfer clock signal output terminal Not used (open)
82	DTRF	O	Writing serial data output terminal Not used (open)
83	APCREF	O	Control signal output to the reference voltage generator circuit for the laser automatic power control
84	LDDR	O	PWM signal output for the laser automatic power control Not used (open)
85	TRDR	O	Tracking servo drive PWM signal (–) output to the BH6511FS (IC303)
86	TFDR	O	Tracking servo drive PWM signal (+) output to the BH6511FS (IC303)
87	DVDD	—	Power supply terminal (+3.3V) (digital system)
88	FFDR	O	Focus servo drive PWM signal (+) output to the BH6511FS (IC303)

Pin No.	Pin Name	I/O	Description
89	FRDR	O	Focus servo drive PWM signal (–) output to the BH6511FS (IC303)
90	FS4	O	Clock signal (176.4 kHz) output terminal (X'tal system) Not used (open)
91	SRDR	O	Sled servo drive PWM signal (–) output to the BH6511FS (IC303)
92	SFDR	O	Sled servo drive PWM signal (+) output to the BH6511FS (IC303)
93	SPRD	O	Spindle servo drive PWM signal (–) output to the BH6511FS (IC303)
94	SPFD	O	Spindle servo drive PWM signal (+) output to the BH6511FS (IC303)
95	FGIN	I	Not used (fixed at "L")
96	TEST1	I	Input terminal for the test (fixed at "L")
97	TEST2	I	
98	TEST3	I	
99	DVSS	—	Ground terminal (digital system)
100	EFMO	O	EFM signal output terminal when recording mode Not used (open)

* I (A) for analog input, O (3) for 3-state output, and O (A) for analog output in the column I/O.

• **SERVO BOARD IC302 CXA2523AR (RF AMP, FOCUS/TRACKING ERROR AMP)**

Pin No.	Pin Name	I/O	Description
1	I	I	I-V converted RF signal I input from the optical pick-up block detector
2	J	I	I-V converted RF signal J input from the optical pick-up block detector
3	VC	O	Middle point voltage (+1.65V) generation output terminal
4 to 9	A to F	I	Signal input from the optical pick-up detector
10	PD	I	Light amount monitor input from the optical pick-up block laser diode
11	APC	O	Laser amplifier output terminal to the automatic power control circuit
12	APCREF	I	Reference voltage input terminal for setting laser power
13	GND	—	Ground terminal
14	TEMPI	I	Connected to the temperature sensor Not used (open)
15	TEMPR	O	Output terminal for a temperature sensor reference voltage Not used (open)
16	SWDT	I	Writing serial data input from the MD mechanism controller (IC501)
17	SCLK	I	Serial data transfer clock signal input from the MD mechanism controller (IC501)
18	XLAT	I	Serial data latch pulse signal input from the MD mechanism controller (IC501)
19	$\overline{\text{XSTBY}}$	I	Standby signal input terminal "L": standby (fixed at "H" in this set)
20	F0CNT	I	Center frequency control voltage input terminal of internal circuit (BPF22, BPF3T, EQ) input terminal
21	VREF	O	Reference voltage output terminal Not used (open)
22	EQADJ	I	Center frequency setting terminal for the internal circuit (EQ)
23	3TADJ	I	Center frequency setting terminal for the internal circuit (BPF3T)
24	VCC	—	Power supply terminal (+3.3V)
25	WBLADJ	I	Center frequency setting terminal for the internal circuit (BPF22)
26	TE	O	Tracking error signal output to the CXD2652AR (IC301)
27	CSLED	I	Connected to the external capacitor for low-pass filter of the sled error signal
28	SE	O	Sled error signal output to the CXD2652AR (IC301)
29	ADFM	O	FM signal output of the ADIP
30	ADIN	I	Receives a ADIP FM signal in AC coupling
31	ADAGC	I	Connected to the external capacitor for ADIP AGC
32	ADFG	O	ADIP duplex signal (22.05 kHz ± 1 kHz) output to the CXD2652AR (IC301)
33	AUX	O	Auxiliary signal (I_3 signal/temperature signal) output terminal Not used (open)
34	FE	O	Focus error signal output to the CXD2652AR (IC301)
35	ABCD	O	Light amount signal (ABCD) output to the CXD2652AR (IC301)
36	BOTM	O	Light amount signal (RF/ABCD) bottom hold output to the CXD2652AR (IC301)
37	PEAK	O	Light amount signal (RF/ABCD) peak hold output to the CXD2652AR (IC301)
38	RF	O	Playback EFM RF signal output to the CXD2652AR (IC301)
39	RFAGC	I	Connected to the external capacitor for RF auto gain control circuit
40	AGCI	I	Receives a RF signal in AC coupling
41	COMPO	O	User comparator output terminal Not used (open)
42	COMPP	I	User comparator input terminal Not used (fixed at "L")
43	ADDC	I	Connected to the external capacitor for cutting the low band of the ADIP amplifier
44	OPO	O	User operational amplifier output terminal Not used (open)
45	OPN	I	User operational amplifier inversion input terminal Not used (fixed at "L")
46	RFO	O	RF signal output terminal
47	MORFI	I	Receives a MO RF signal in AC coupling
48	MORFO	O	MO RF signal output terminal

• **SERVO BOARD IC501 CXP84340-217Q (MD MECHANISM CONTROLLER)**

Pin No.	Pin Name	I/O	Description
1 to 5	TIN3 to TIN7	I/O	Input of the 4×8 matrix test keys (“L” is always output, except in test mode) Not used (open)
6	LOAD	O	Loading motor control signal output to the motor driver (IC305) “H” active *1
7	EJECT	O	Loading motor control signal output to the motor driver (IC305) “H” active *1
8, 9	NCO	O	Not used (open)
10	MDMON	O	Power supply on/off control signal output of the MD mechanism deck section main power supply and loading motor drive (IC305) power supply “H”: power on
11	$\overline{\text{E-SW}}$	I	Inputs the disc loading completion detect switch detection signal “L”: When completed of the disc loading operation
12	AG-OK	O	Output of aging status in test mode “L”: under aging, “H”: aging completed Not used (open)
13	ADJ-OK	O	Output of status when aging completed in test mode “L”: aging NG, “H”: aging OK Not used (open)
14 to 17	NCO	O	Not used (open)
18	DFCTSEL	I	Select whether defect function is used for the CXD2652AR (IC301) “L”: used this function , “H”: not used this function (fixed at “H” in this set)
19	DPLLSEL	I	Select whether digital PLL function is used for the CXD2652AR (IC301) “L”: used this function , “H”: not used this function (fixed at “H” in this set)
20	EMPHSEL	I	Select whether emphasis signal output from pin or unilink data “L”: outputs from both pin and unilink data, “H”: output from pin only (fixed at “H” in this set)
21	LOCK	O	Mini-disc lock detection signal output to the master controller (IC501) “H”: lock
22	NCO	O	Not used (open)
23	2M/$\overline{\text{4M}}$	I	Select whether D-RAM capacitance 2M bit or 4M bit “L”: 4M bit (external D-RAM) , “H”: 2M bit (internal D-RAM of CXD2652AR) (fixed at “L” in this set)
24, 25	NCO	O	Not used (open)
26	MNT0	I	Focus OK signal input from the CXD2652AR (IC301) “H” is input when focus is on (“L”: NG)
27	MNT1	I	Track jump detection signal input from the CXD2652AR (IC301)
28	MNT2	I	Busy monitor signal input from the CXD2652AR (IC301)
29	MNT3	I	Spindle servo lock status monitor signal input from the CXD2652AR (IC301)
30	$\overline{\text{RESET}}$	I	System reset signal input from the master controller (IC501), reset signal generator (IC652) and reset switch (SW503) “L”: reset For several hundreds msec. after the power supply rises, “L” is input, then it changes to “H”
31	EXTAL	O	Main system clock output terminal (10 MHz)
32	XTAL	I	Main system clock input terminal (10 MHz)
33	VSS	—	Ground terminal
34	TX	O	Sub system clock output terminal (32.768 kHz) Not used (open)
35	TEX	I	Sub system clock input terminal (32.768 kHz) Not used (fixed at “L”)
36	AVSS	—	Ground terminal (for A/D converter)
37	AVREF	I	Reference voltage input terminal (+5V) (for A/D converter)
38	INIT	I	Initial reset signal input terminal (A/D input) (fixed at “H”)
39	TEMP	I	Temperature sensor (TH501) input terminal (A/D input)
40	ACNT	I	Select the number of load/eject aging times (A/D input) 0H – 54H (30 times), 55H – OA9H (20 times), OAAH – OFFH (10 times)
41	DO-SEL	I	Select the digital output bits (A/D input)
42	EE-CS	O	Chip select signal output to the external EEPROM device Not used (open)
43	EE-CKO	O	Serial data transfer clock signal output to the external EEPROM device Not used (open)
44	EE-SIO	I/O	Two way data bus with the external EEPROM device Not used (open)
45	MD-SO	O	Writing serial data signal output to the CXD2652AR (IC301) and CXA2523AR (IC302)
46	LINKOFF	O	Unilink on/off control signal output for the SONY bus “L”: link on, “H”: link off

Pin No.	Pin Name	I/O	Description
47	UNIREQ	O	Data request signal output terminal (for SONY bus) "H": request on Not used (open)
48	UNICKIO	I/O	Serial clock signal input from the master controller (IC501) or serial clock signal output to the SONY bus interface (IC701) and master controller (IC501) (for SONY bus)
49	UNISI	I	Serial data input from the SONY bus interface (IC701)
50	UNISO	O	Serial data output to the SONY bus interface (IC701)
51	MD-CKO	O	Serial data transfer clock signal output to the CXD2652AR (IC301) and CXA2523AR (IC302)
52	MD-SI	I	Reading serial data signal input from the CXD2652AR (IC301)
53	NCO	O	Not used (open)
54	SENS	I	Internal status (SENSE) input from the CXD2652AR (IC301)
55	CC-XINT	I	Interrupt status input from the CXD2652AR (IC301)
56	$\overline{\text{LIMIT-IN}}$	I	Detection input from the sled limit-in detect switch The optical pick-up is inner position when "L"
57	EJT-KEY	I	Eject request signal input terminal "L": eject on Not used (fixed at "H")
58	ERROR-PWM	O	PWM error monitor output terminal (C1and ATER is output when test mode) Not used (open)
59	$\overline{\text{MD-RST}}$	O	Reset signal output to the PCM1718E (IC101), CXD2652AR (IC301) and BH6511FS (IC303) "L": reset
60	BU-IN	I	Battery detect signal input from the SONY bus interface (IC600) and battery check circuit "H": battery on
61	$\overline{\text{BUS-ON}}$	I	SONY bus on/off control signal input from the master controller (IC700) "L": bus on
62	SQSY	I	Subcode Q sync (SCOR) input from the CXD2652AR (IC301) "L" is input every 13.3 msec Almost all, "H" is input
63	$\overline{\text{C-SW}}$	I	Inputs the disc loading start or disc eject completion detect switch detection signal "L": When start or eject completed of the disc loading operation
64	MD-LAT	O	Serial data latch pulse signal output to the CXD2652AR (IC301) and CXA2523AR (IC302)
65	MD-ON	O	Power supply on/off control signal output of the MD mechanism deck section main power supply "H": power on
66	DEEMP	O	Emphasis on/off control signal output to the PCM1718E (IC101) "H": emphasis on
67	A-MUTE	O	Audio muting on/off control signal output terminal
68	NCO	O	Not used (open)
69	TSTCKO	O	Output of clock signal for the test mode display Not used (open)
70	TSTSO	O	Output of data for the test mode display Not used (open)
71	$\overline{\text{TSTMOD}}$	I	Setting terminal for the test mode "L": test mode, "H": normal mode
72	VCC	—	Power supply terminal (+5V)
73	NIL	I	Not used (fixed at "H")
74 to 77	TOUT0 to TOUT3	O	Output of the 4×8 matrix test keys Not used (open)
78 to 80	TIN0 to TIN2	I/O	Input of the 4×8 matrix test keys ("L" is always output, except in test mode) Not used (open)

*1 Loading motor (M903) control

Operation / Terminal	IN	OUT	BRAKE	STOP
LOAD (pin ⑥)	"H"	"L"	"H"	"L"
EJECT (pin ⑦)	"L"	"H"	"H"	"L"

• **MAIN BOARD IC501 MB90574PMT-G-266-BND (MASTER CONTROLLER)**

Pin No.	Pin Name	I/O	Description
1	TUNON	O	Tuner system power supply on/off control signal output to the BA4908 (IC671) "H": tuner power on
2	ANT CUT	O	Tuner system power supply on/off control signal output terminal "H": tuner power on Not used (open)
3	$\overline{\text{BUSON}}$	O	Bus on/off control signal output to the MD mechanism controller (IC501) and SONY bus interface (IC701) "L": bus on
4 to 6	NCO	O	Not used (open)
7	ILLON	O	Power on/off control signal output of the illumination LED and liquid crystal display driver (IC901) "H": power on
8	VCC	—	Power supply terminal (+5V)
9	E2P SIO	I/O	Two-way data E2P bus with the FM/AM tuner unit (TU1)
10	E2P CKO	O	E2P bus clock signal output to the FM/AM tuner unit (TU1)
11	$\overline{\text{SYSRST}}$	O	System reset signal output to the MD mechanism controller (IC501) and SONY bus interface (IC701) "L": reset
12	$\overline{\text{DOORSW}}$	I	Front panel open/close detection signal input terminal "L" is input when the front panel is closed
13	LCDSO	O	Serial data output to the liquid crystal display driver (IC901)
14	LCDCKO	O	Serial data transfer clock signal output to the liquid crystal display driver (IC901)
15	LCDCE	O	Chip enable signal output to the liquid crystal display driver (IC901) "H" active
16	BEEP	O	Beep sound drive signal output to the power amplifier (IC611)
17	UNISI	I	Serial data input from the SONY bus interface (IC701)
18	UNISO	O	Serial data output to the SONY bus interface (IC701)
19	UNICKO	O	Serial clock signal output to the MD mechanism controller (IC501) and SONY bus interface (IC701)
20	UNICKI	I	Serial clock signal input from the MD mechanism controller (IC501) (for SONY bus)
21	CD MD	I	Setting terminal for the internal mechanism CD or MD "L": CD, "H": MD (fixed at "H" in this set)
22	$\overline{\text{FLASHW}}$	I	Internal flash memory data write mode detection signal input terminal "L": data write mode Not used
23	NCO	O	Not used (open)
24	SIRCS	I	Sircs remote control signal input from the remote control receiver (IC951)
25 to 28	NCO	O	Not used (open)
29	DOORIND	O	LED drive signal output of the MD disc slot illumination and ⏏ indicator (LED810, LSW810) "H": LED on "H" is output to turn on LED when front panel is opened
30, 31	NCO	O	Not used (open)
32	NS MASK	O	Discharge control signal output for the noise detection circuit "H": discharge
33	VSS	—	Ground terminal
34	C	—	Connected to coupling capacitor for the power supply
35	$\overline{\text{AD ON}}$	O	A/D converter power control signal output terminal When the KEYACK (pin ⑯) that controls reference voltage power for key A/D conversion input is active, "L" is output from this terminal to enable the input
36	REIN0	I	Dial pulse input of the rotary encoder (RE901) (for VOLUME/BASS/TREBLE/BALANCE/FADER control)
37	REIN1	I	
38	DVCC	—	Power supply terminal (+5V) (for D/A converter)
39	DVSS	—	Ground terminal (for D/A converter)
40, 41	NCO	O	Not used (open)
42	AVCC	—	Power supply terminal (+5V) (for analog system)

Pin No.	Pin Name	I/O	Description
43	AVRH	I	Reference voltage (+5V) input terminal (for A/D converter)
44	AVRL	I	Reference voltage (0V) input terminal (for A/D converter)
45	AVSS	—	Ground terminal (for analog system)
46	KEYIN0	I	Key input terminal (A/D input) (LSW901 to LSW908, S901 to S904) OFF, SOURCE, SOUND, MENU, PTY DSPL, LIST, ENTER, MODE, SEEK/AMS - ⏮ ◀◀ + ▶▶⏭ ▶▶, DISC/PRST +, PRST/DISC - keys input
47	KEYIN1	I	Key input terminal (A/D input) (LSW810, LSW909 to LSW917) ⏏, D-BASS, TA, FA, 6 to 3 SHUF 2, REP 1 keys input
48	RCIN0	I	Rotary remote commander key input terminal (A/D input)
49	DSTSEL	I	Destination setting terminal (fixed at "L" in this set)
50	QUALITY	I	Noise level detection signal input at SEEK mode (A/D input)
51	FMAGC	I	FM AGC detection signal input from the FM/AM tuner unit (TU1) (A/D input)
52	MPTH	I	Multi-path detection signal input from the RDS decoder (IC51) (A/D input)
53	VSM	I	FM and AM signal meter voltage detection input from the FM/AM tuner unit (TU1) (A/D input)
54	VCC	—	Power supply terminal (+5V)
55	RAMBU	I	Internal RAM reset detection signal input terminal Input terminal to check that RAM data are not destroyed due to low voltage This checking is made within 100 msec after reset Not used (fixed at "H")
56	TUNATT	O	Muting on/off control signal output of the FM/AM tuner signal "H": muting on
57	$\overline{\text{VOLATT}}$	O	Pre amplifier muting on/off control signal output to the electrical volume (IC151) "L": muting on
58	ATT	O	Audio line muting on/off control signal output terminal "H": muting on
59	AMPON	O	Standby on/off control signal output to the power amplifier (IC611) "L": standby mode, "H": ampifier on
60	$\overline{\text{AMPATT}}$	O	Power amplifier muting on/off control signal output to the power amplifier (IC611) "L": muting on
61	COLSW	I	Setting terminal for the illumination color "L": 2 color, "H": 1 color (fixed at "H" in this set)
62	COLSEL	I	Setting terminal for the illumination color "L": amber, "H": green (fixed at "L" in this set)
63	VSS	—	Ground terminal
64	DAVN	I	Data transmit completed detection signal input from the RDS decoder (IC51) "H" active
65	FILE	I	Setting terminal for the custom file "L": unavailable, "H": available (fixed at "H" in this set)
66	TEXT	I	Setting terminal for the CD text "L": unavailable, "H": available (fixed at "H" in this set)
67	$\overline{\text{NOSESW}}$	I	Front panel block remove/attach detection signal input from the nose detection switch (SW504) "L": front panel is attached
68, 69	NCO	O	Not used (open)
70	I2C SIO	I/O	Two-way data I2C bus with the FM/AM tuner unit (TU1), RDS decoder (IC51) and electrical volume (IC151)
71	I2C CKO	O	I2C bus clock signal output to the FM/AM tuner unit (TU1), RDS decoder (IC51) and electrical volume (IC151)
72	NCO	O	Not used (open)
73	X1A	O	Sub system clock output terminal (32.768 kHz)
74	X0A	I	Sub system clock input terminal (32.768 kHz)
75	NCO	O	Not used (open)
76	KEYACK	I	Input of acknowledge signal for the key entry Acknowledge signal is input to accept function and eject keys in the power off status On at input of "H"
77	BUIN	I	Battery detection signal input from the SONY bus interface (IC701) and battery detect circuit "L" is input at low voltage

Pin No.	Pin Name	I/O	Description
78	ILLIN	I	Auto dimmer control illumination line detection signal input terminal "H" is input at dimmer detection Not used (fixed at "L")
79	TELATT	I	Telephone detection signal input terminal At input of "H", the signal is attenuated by –20 dB Used for the MDX-C6500R/C6500RX only (MDX-C6400R: fixed at "L")
80	NCO	O	Not used (open)
81	$\overline{\text{TEST IN}}$	I	Setting terminal for the test mode "L": test mode, Normally: fixed at "H"
82	$\overline{\text{ACC IN}}$	I	Accessory detection signal input terminal "L": accessory on
83	NCO	O	Not used (open)
84	LOCKIN	I	Mini-disc lock detection signal input from the MD mechanism controller (IC501) "H": lock
85	$\overline{\text{RCIN1}}$	I	Rotary remote commander shift key input terminal "L": shift
86	HSTX	I	Hardware standby input terminal "L": hardware standby mode Reset signal input in this set
87	MD2	I	Setting terminal for the CPU operational mode (fixed at "L" in this set)
88	MD1	I	Setting terminal for the CPU operational mode (fixed at "H" in this set)
89	MD0	I	Setting terminal for the CPU operational mode (fixed at "H" in this set)
90	$\overline{\text{RSTX}}$	I	System reset signal input from the reset signal generator (IC652) and reset switch (SW503) "L": reset "L" is input for several 100 msec after power on, then it changes to "H"
91	VSS	—	Ground terminal
92	X0	I	Main system clock input terminal (3.68 MHz)
93	X1	O	Main system clock output terminal (3.68 MHz)
94	VCC	—	Power supply terminal (+5V)
95 to 97	NCO	O	Not used (open)
98	DIM SEL	I	Setting terminal for the dimmer "L": dimmer in, "H": no dimmer (fixed at "H" in this set)
99	TAP CD	I	Setting terminal for the internal mechanism tape or CD "L": CD, "H": tape (fixed at "L" in this set)
100, 101	NCO	O	Not used (open)
102	$\overline{\text{AMTL IN}}$	I	Auto metal detection signal input terminal "L": auto metal Not used (open)
103	AMS IN	I	Input terminal of whether a music is present or not is detected at auto music sensor "L": music is present, "H": music is not present Not used (open)
104	REEL	I	Rotation detect signal input terminal Not used (open)
105	POS0	I	Tape position (EJECT/FF/REW/REV/ FWD mode) detect input from the tape operation switch on the deck mechanism Not used this function (open) POS0: "L": EJECT mode, "H": others mode POS1: "L": FF and FWD mode, "H": others mode POS2: "L": REW mode, "H": others mode POS3: "L": REV and EJECT mode, "H": others mode
106	POS1	I	
107	POS2	I	
108	POS3	I	
109	LM EJ	O	Loading motor control signal output terminal "H" active (For the eject direction and reverse side operation) Not used (open)
110	LM LD	O	Loading motor control signal output terminal "H" active (For the loading direction and forward side operation) Not used (open)
111	CM ON	O	Capstan/reel motor control signal output terminal "H": motor on Not used (open)
112	TAPON	O	Tape system power supply on/off control signal output terminal "H": tape on Not used (open)
113	N ROUT	O	Forward/reverse direction control signal output terminal "L": forward direction, "H": reverse direction Not used (open)
114	AMSON	O	Tape auto music sensor control signal output terminal "L" is output to lower the gain for audio level at FF/REW mode Not used (open)
115	MTLON	I/O	METAL control in/out terminal At initial mode: auto/manual mode selection input of METAL function (manual at "L" input) At manual mode: METAL on/off control signal output terminal (METAL on at "H" output) Not used this function (open)

Pin No.	Pin Name	I/O	Description
116	DOLON	I/O	Dolby control in/out terminal At initial mode: valid/invalid selection input of dolby function (valid at “L” input) At normal mode: dolby on/off control signal output terminal (dolby on at “H” output) Not used this function (open)
117	TAPATT	O	Audio signal select control signal output terminal Not used (open)
118	NCO	O	Not used (open)
119	VSS	—	Ground terminal
120	PW ON	O	Main system power supply on/off control signal output to the BA4908 (IC671) “H”: power on